

FIG. 1

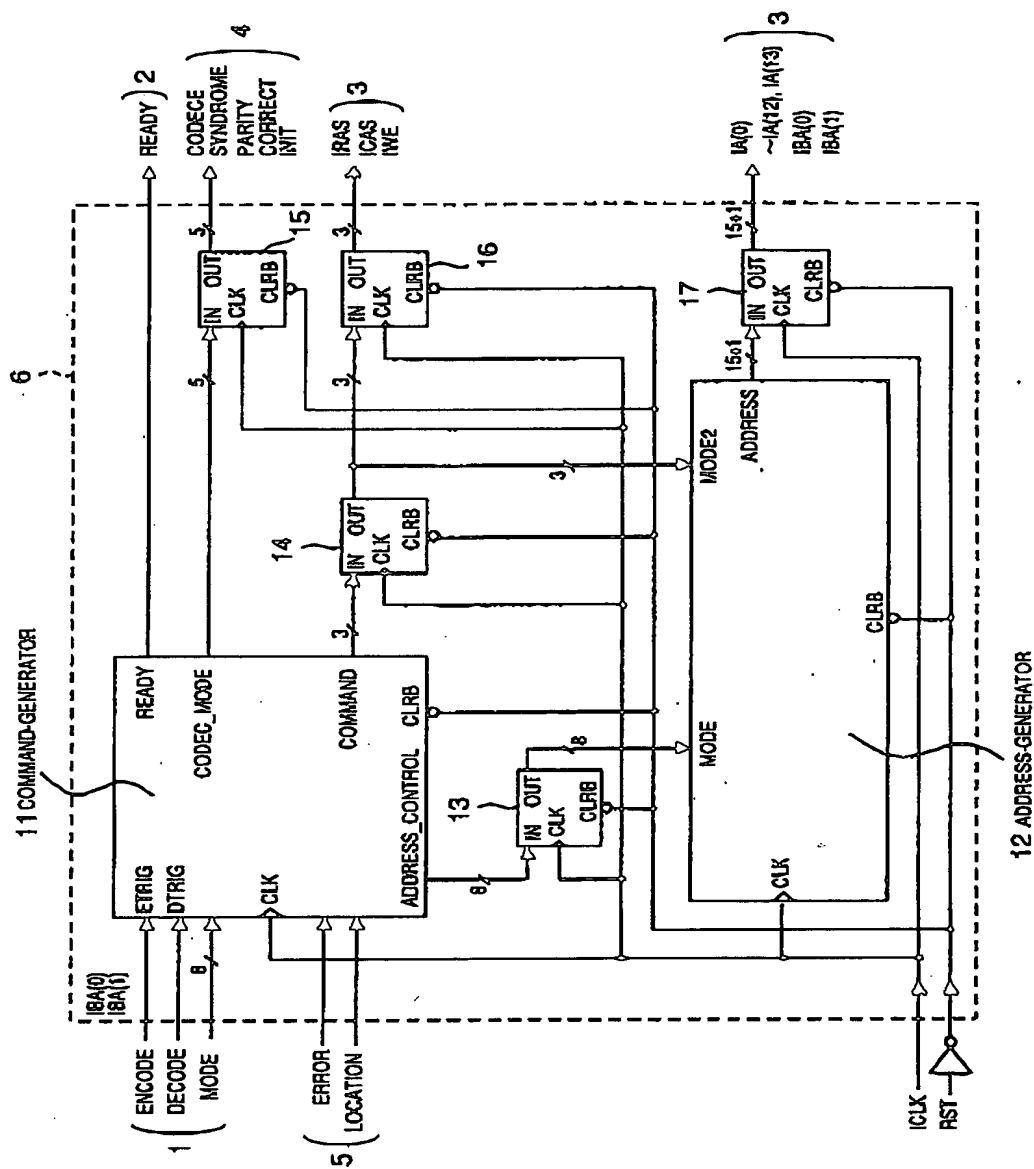


FIG. 3

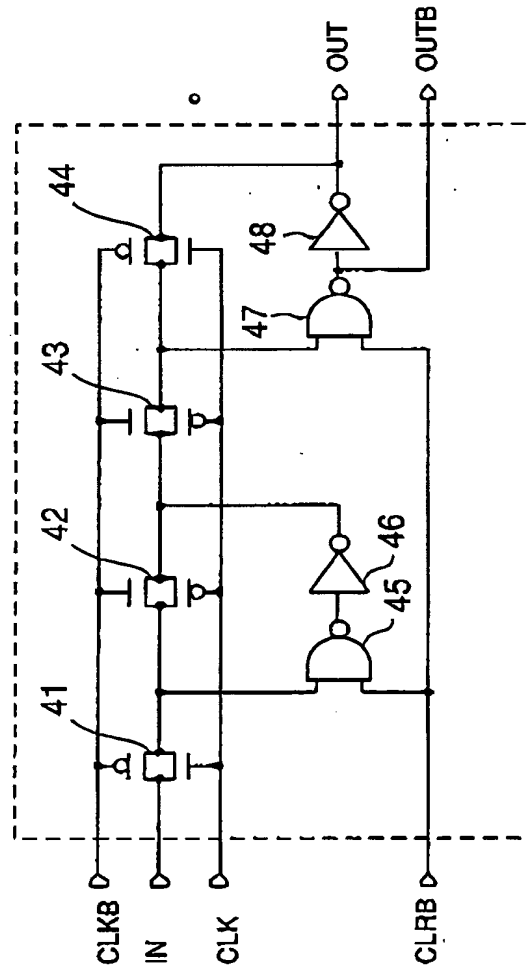


FIG. 4B

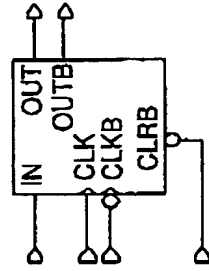


FIG. 4A

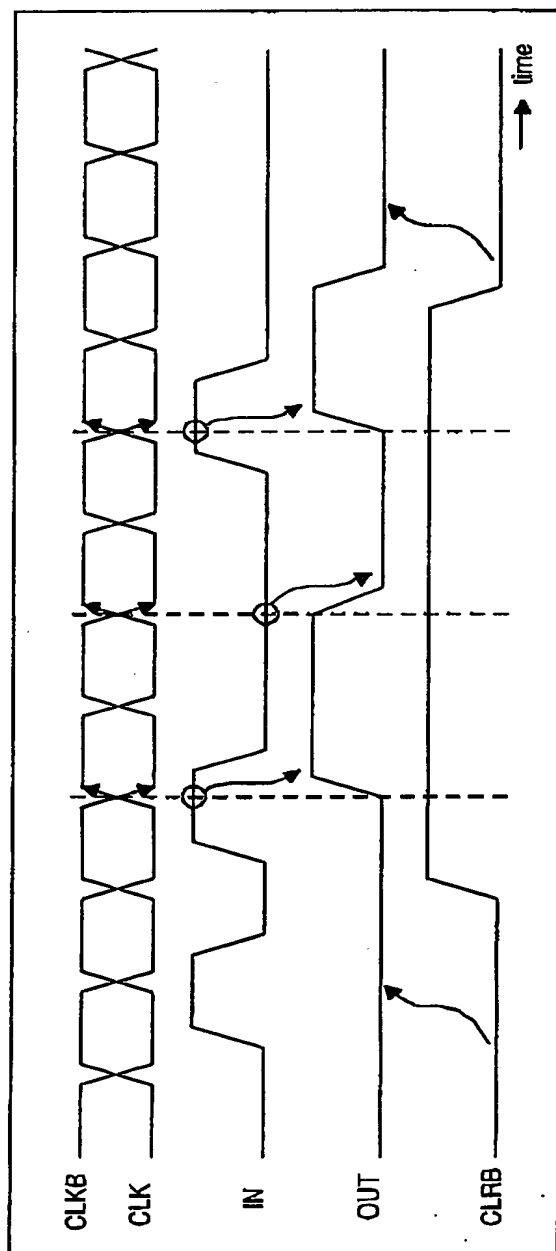
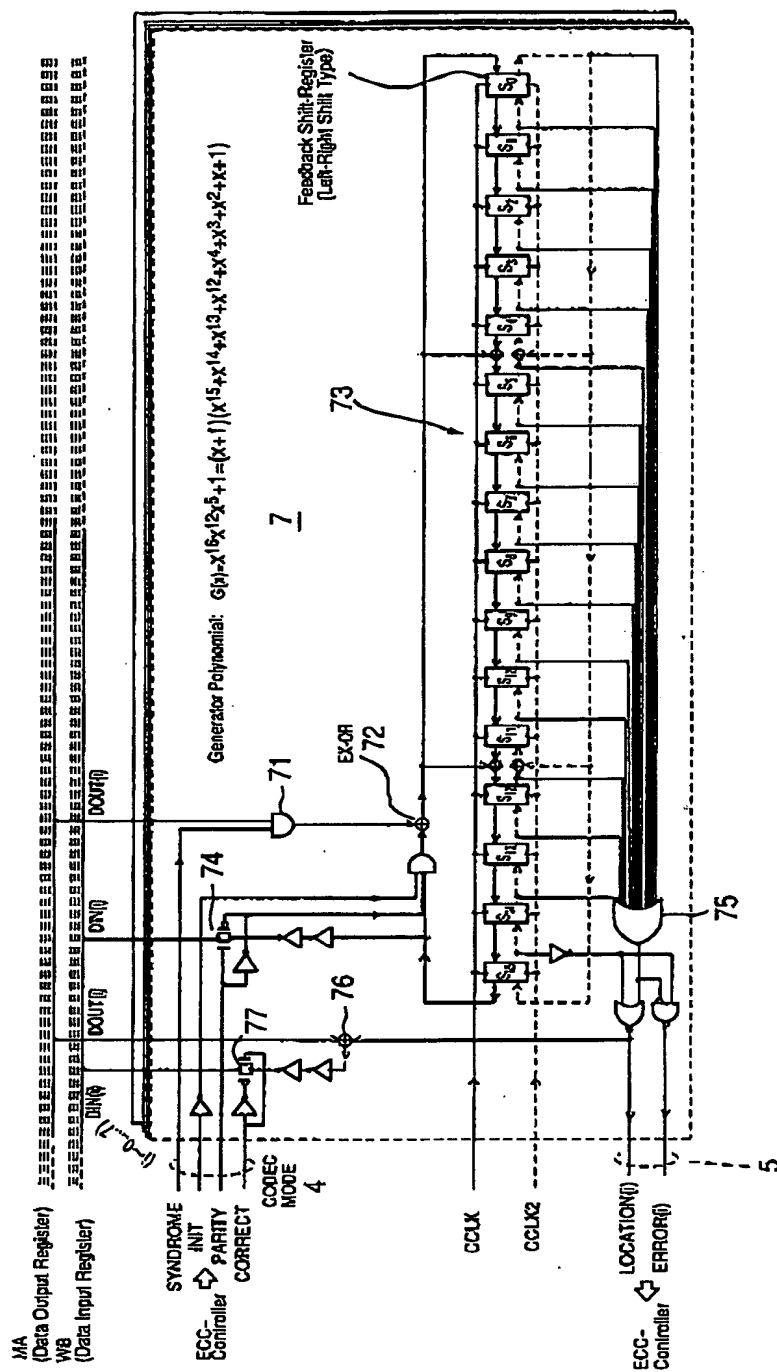
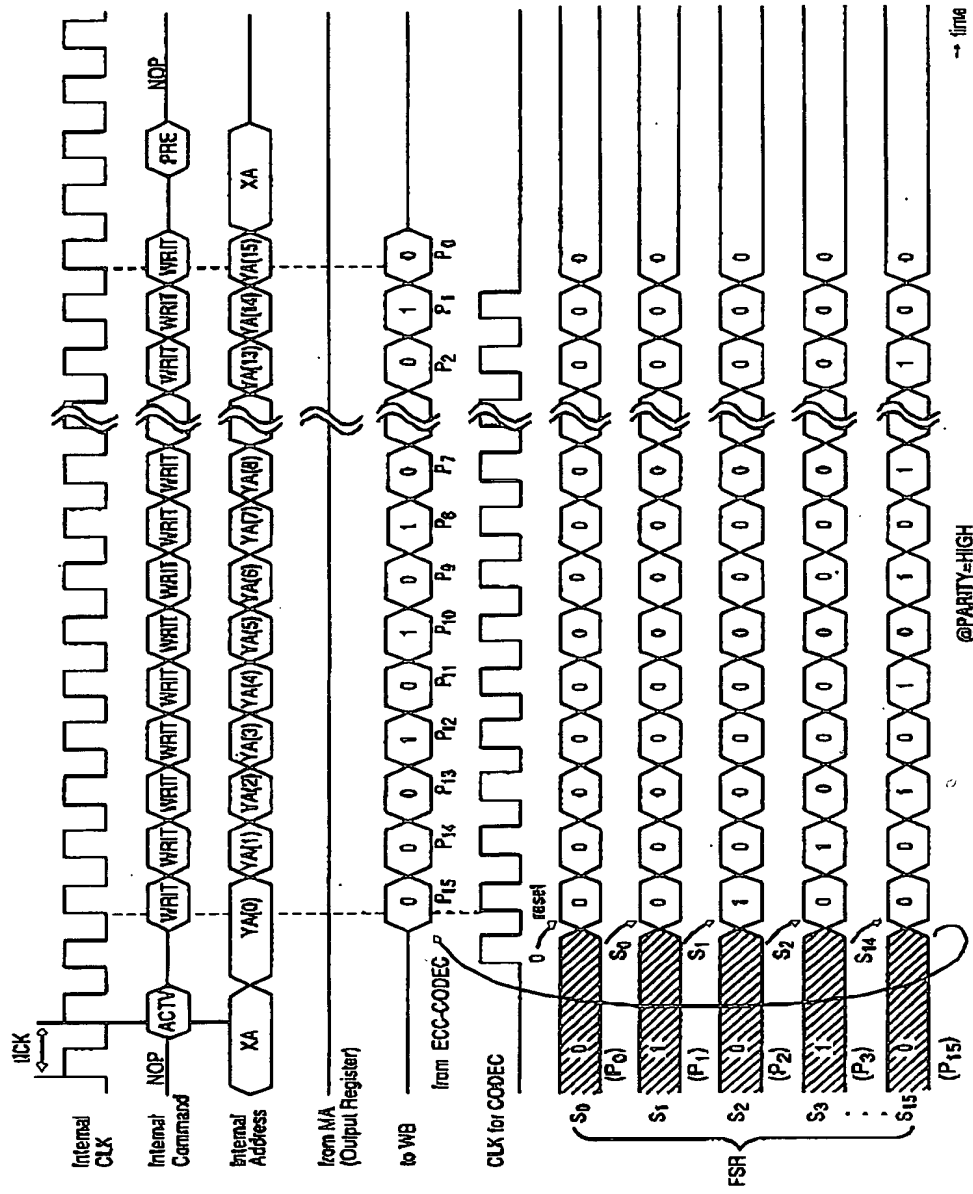


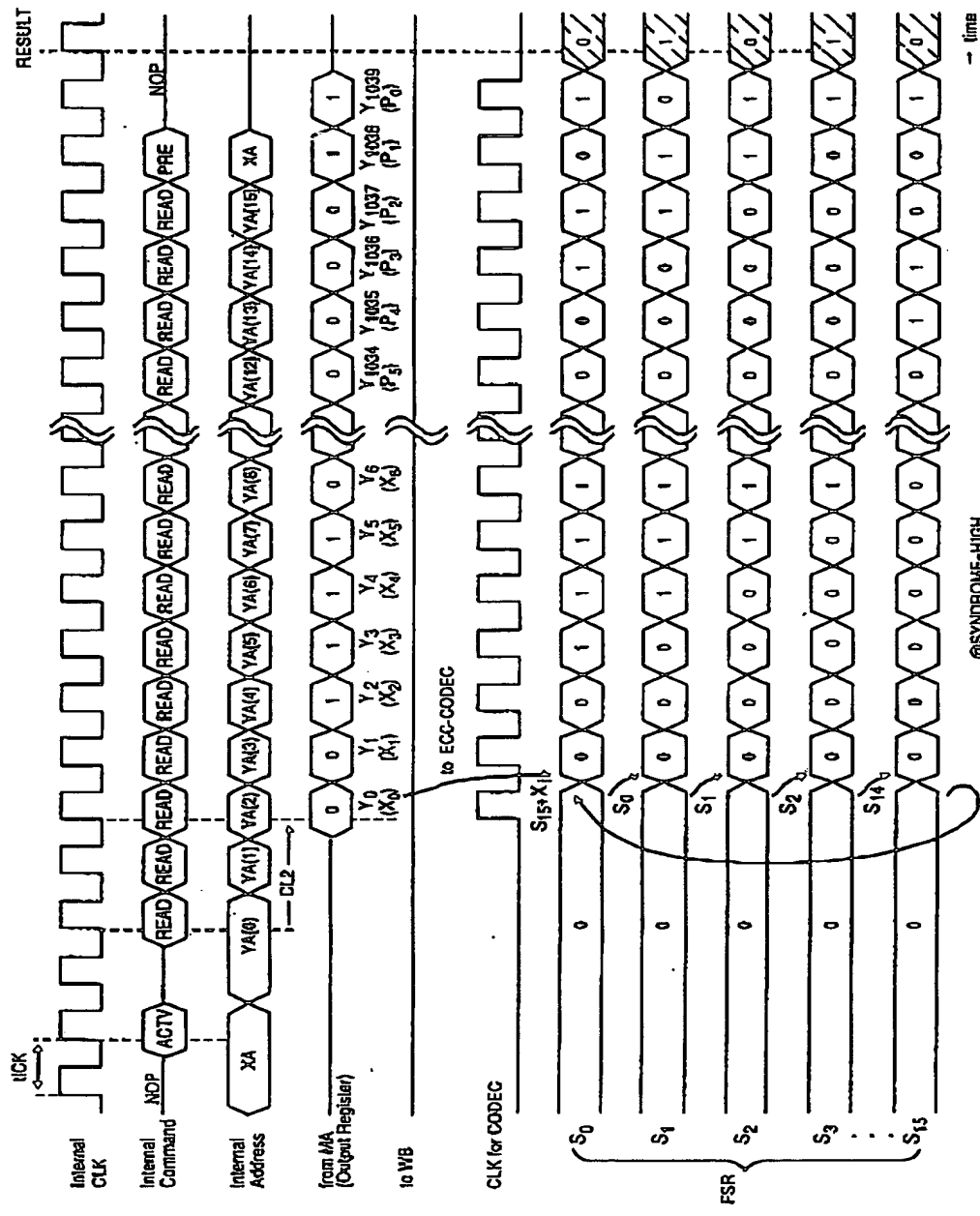
FIG. 5





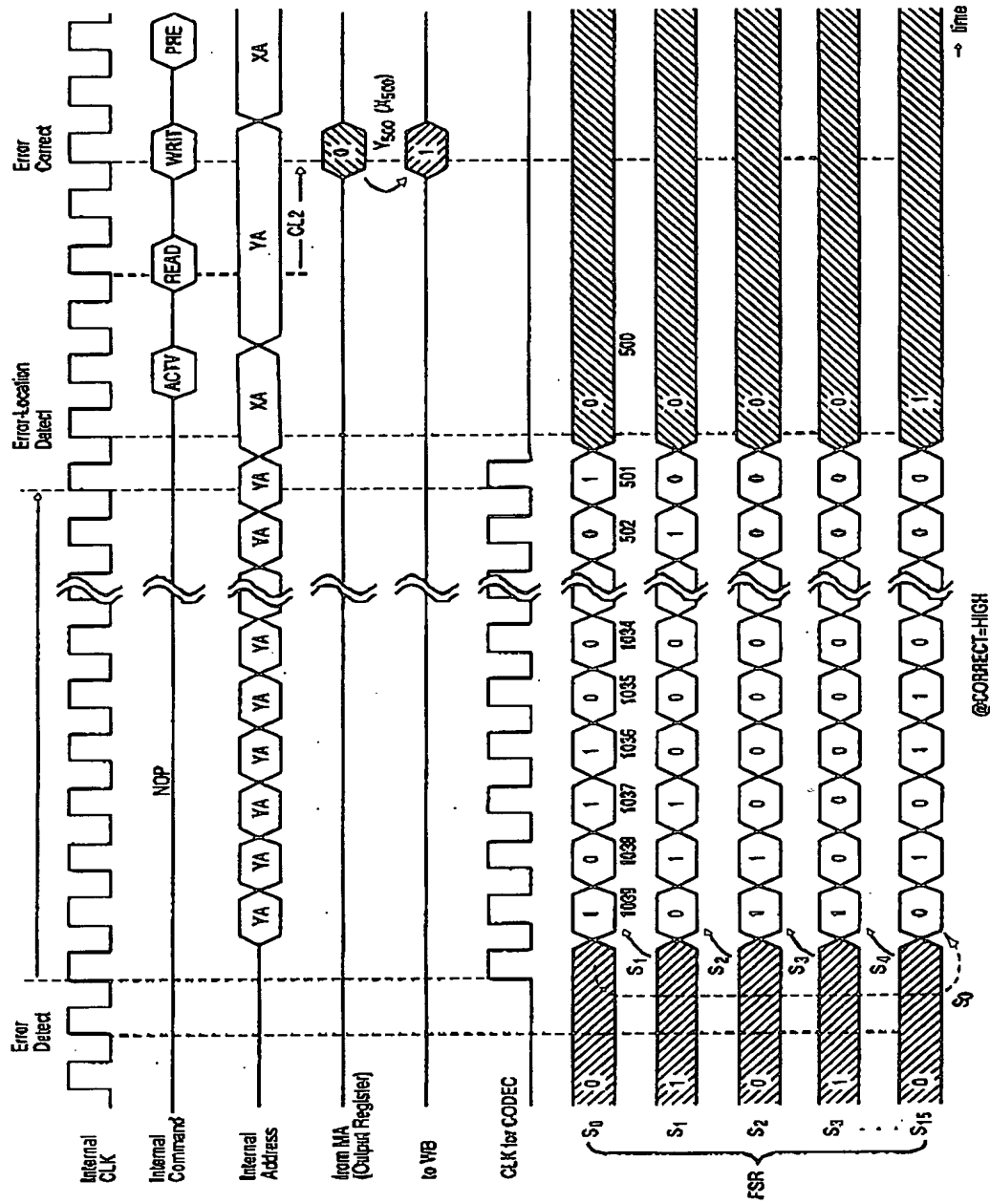
Example 1 of Super Self-Refresh Internal Operation
(Parity-Generation (2) Parity Bit Writing)

FIG. 8



Example 2 of Super Self-Refresh Internal Operation
(Correct (1) Syndrome Calculation)

FIG. 9



Example 2 of Super Self-Refresh Internal Operation
(Correct (2) Error Location Detection and Correction/Writing)

FIG. 10

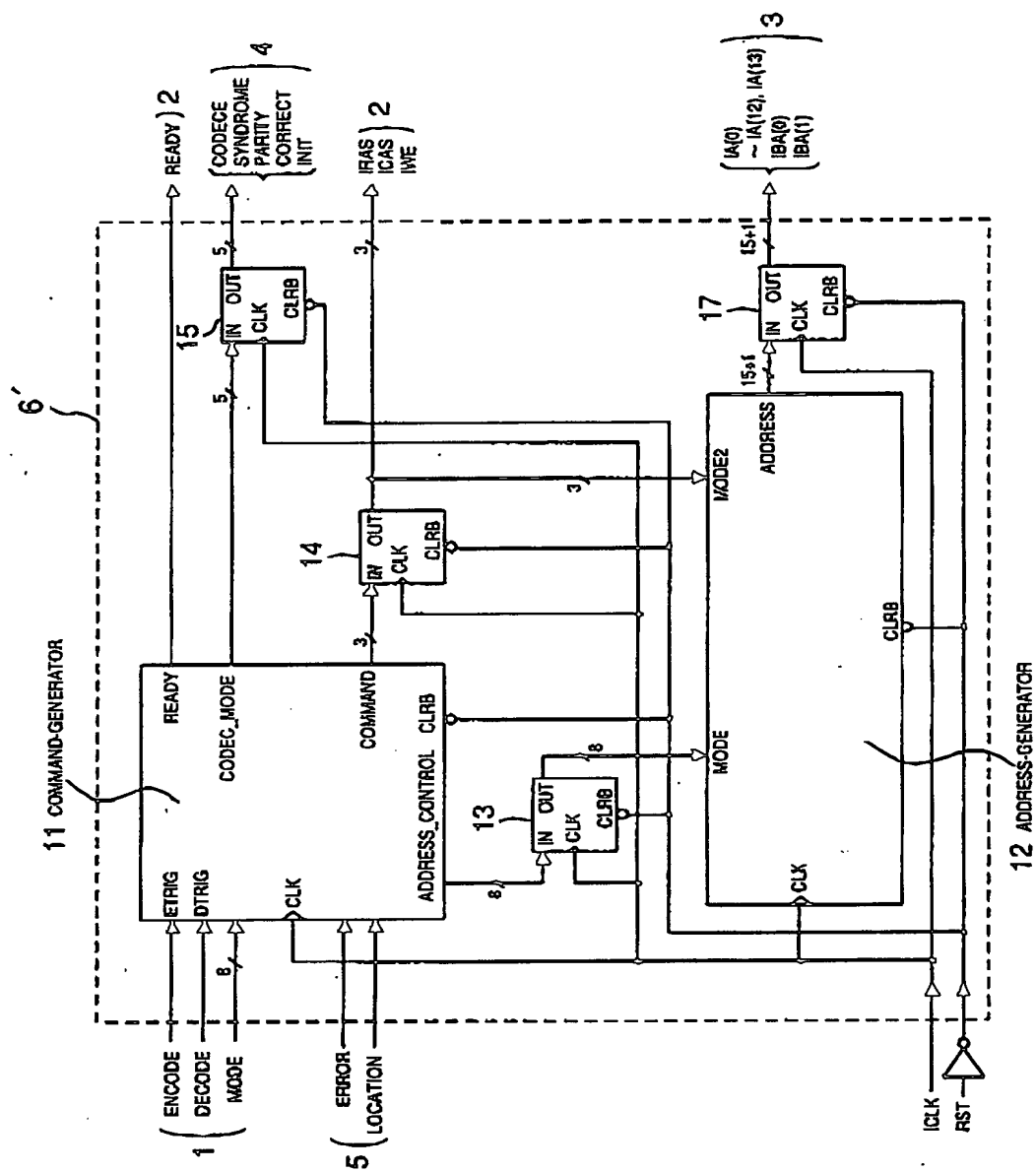


FIG. 11

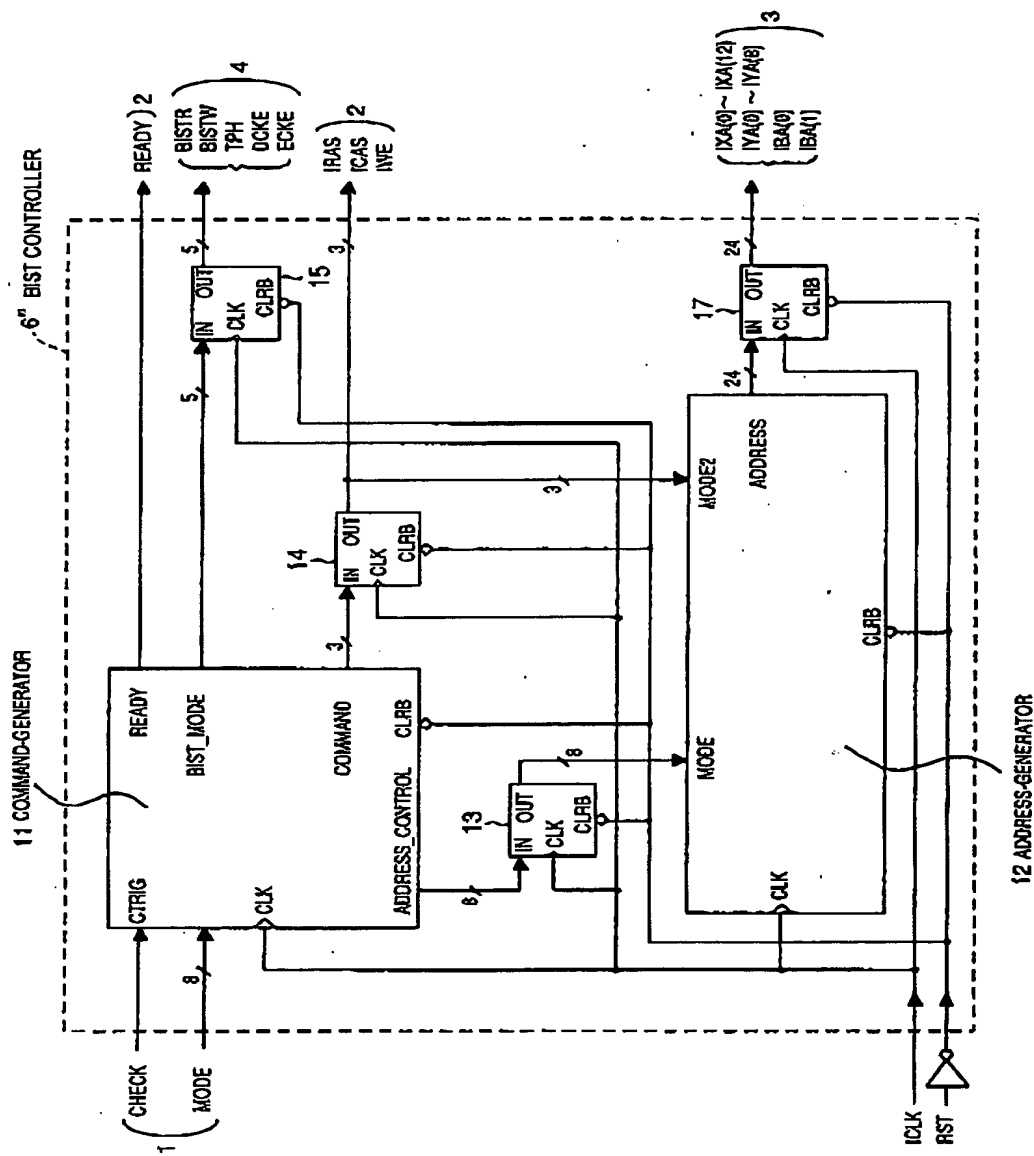
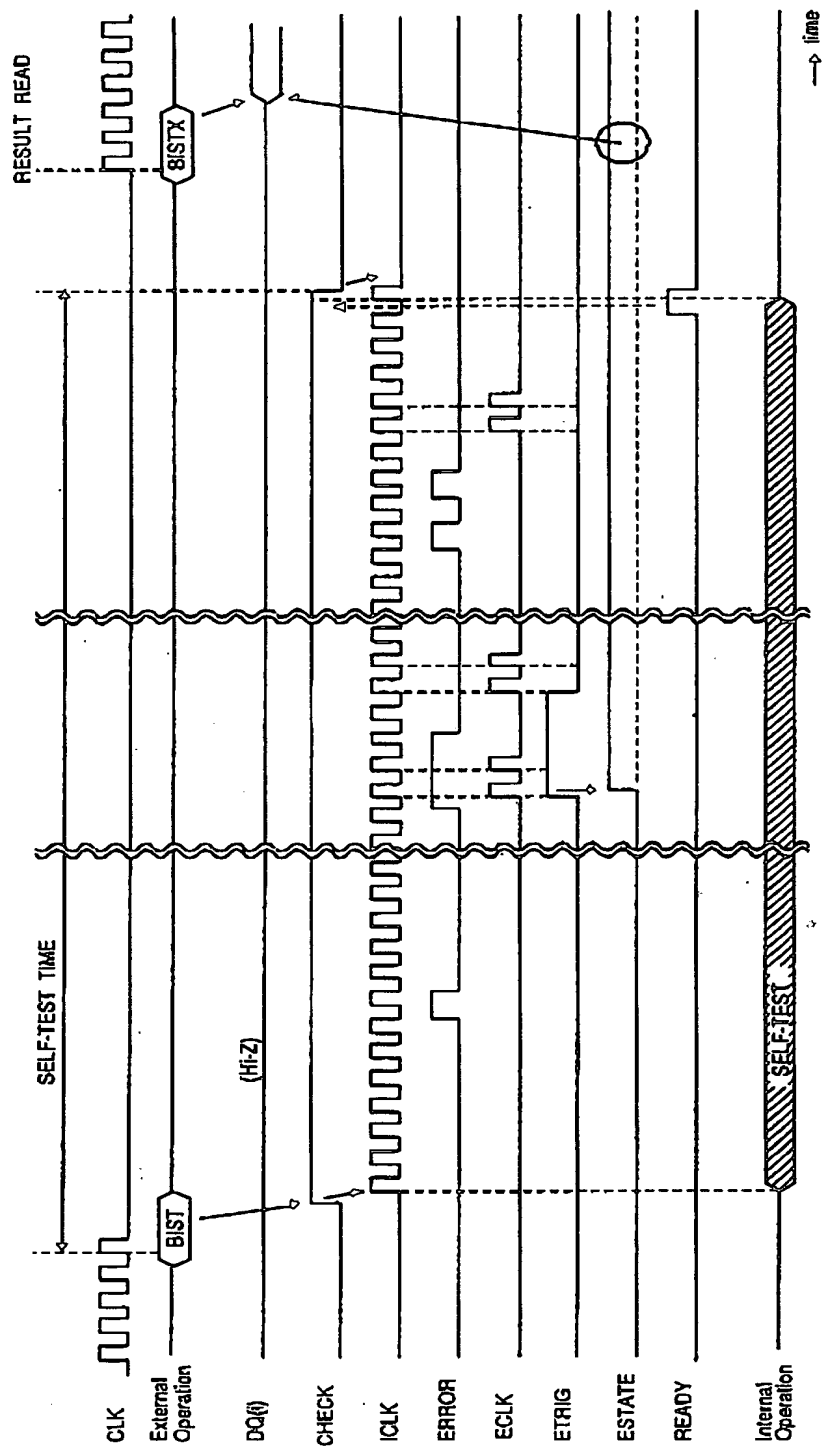


FIG. 12



Operation Sequence of BIST

FIG. 13

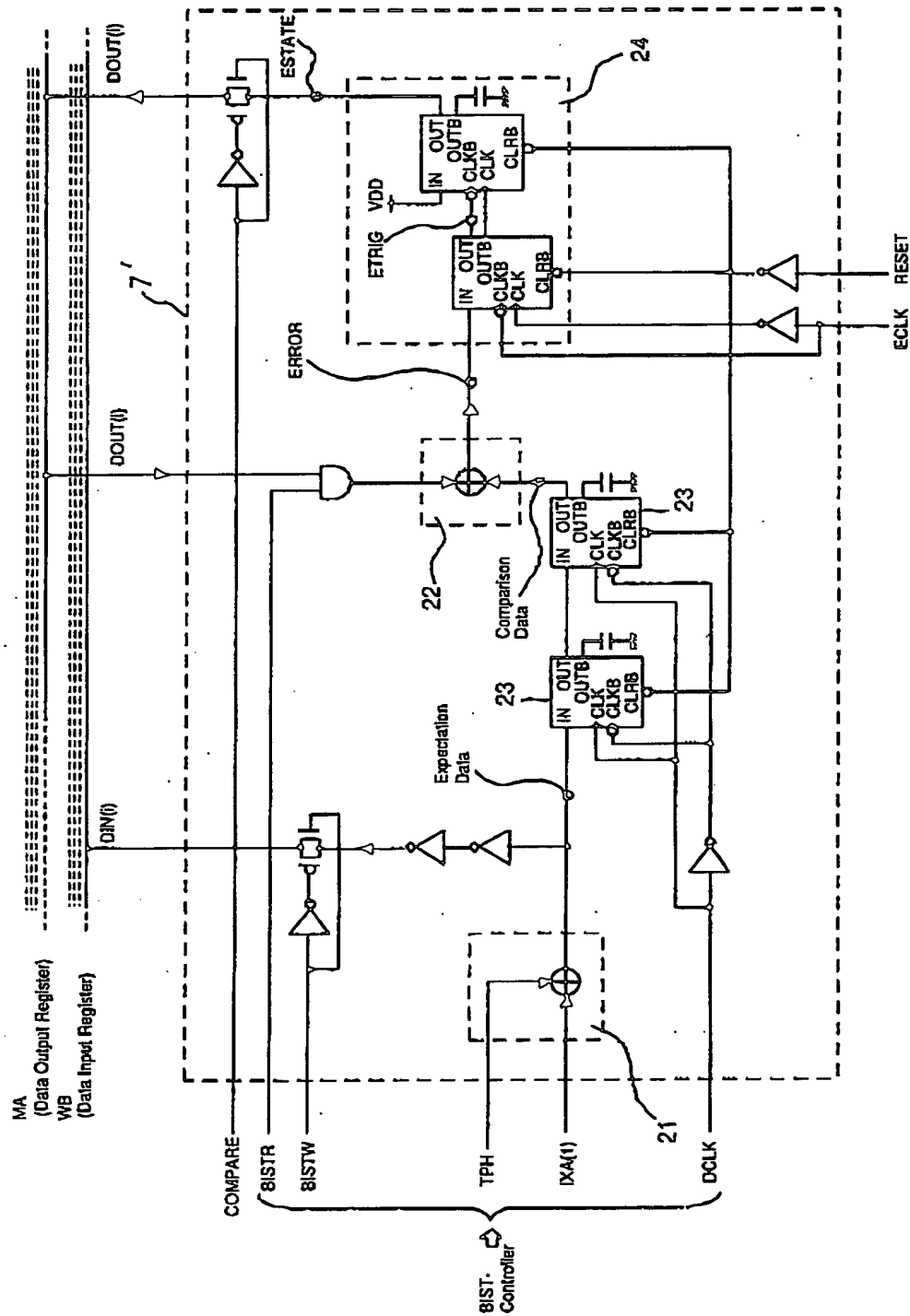


FIG. 14

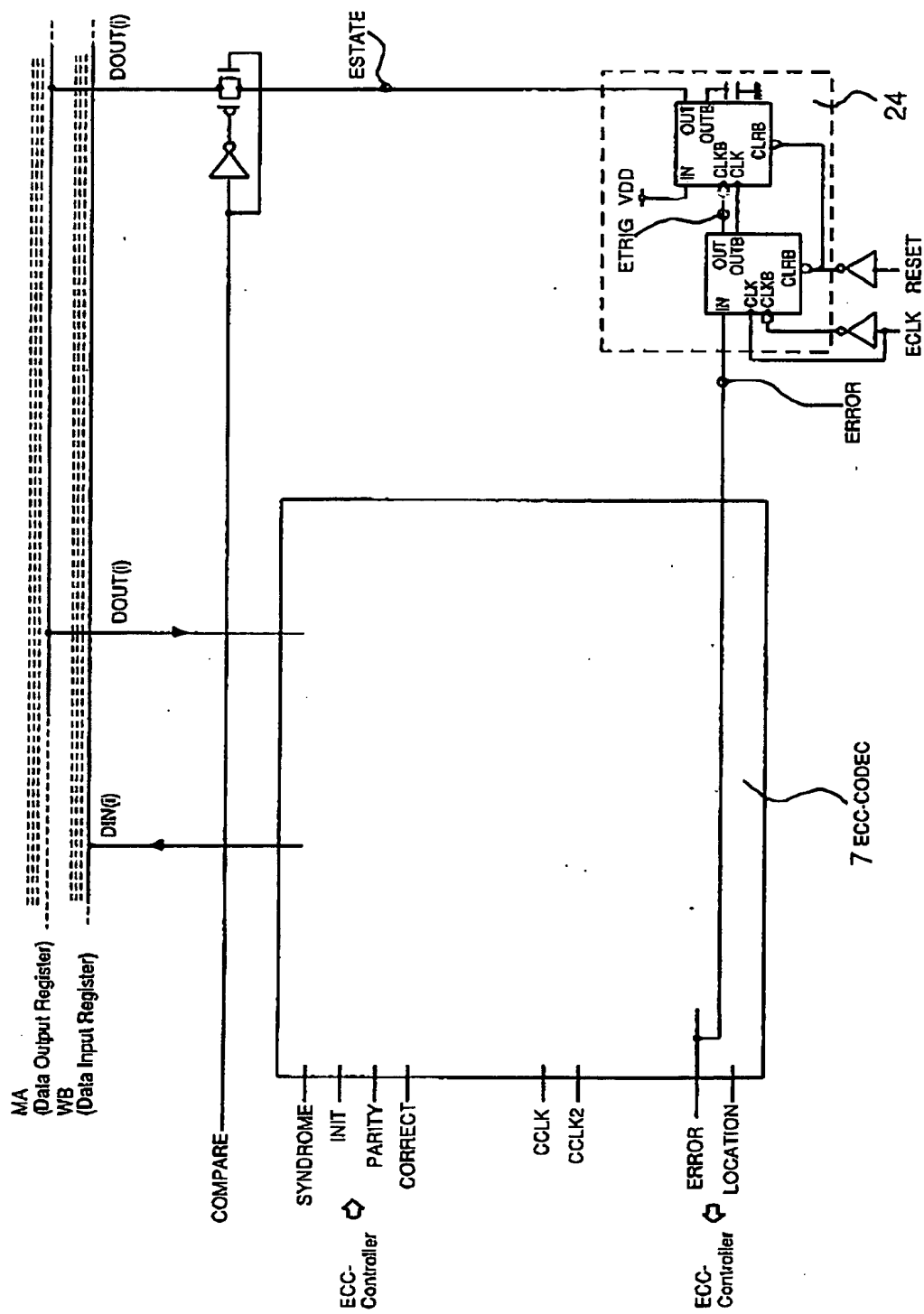


FIG. 15

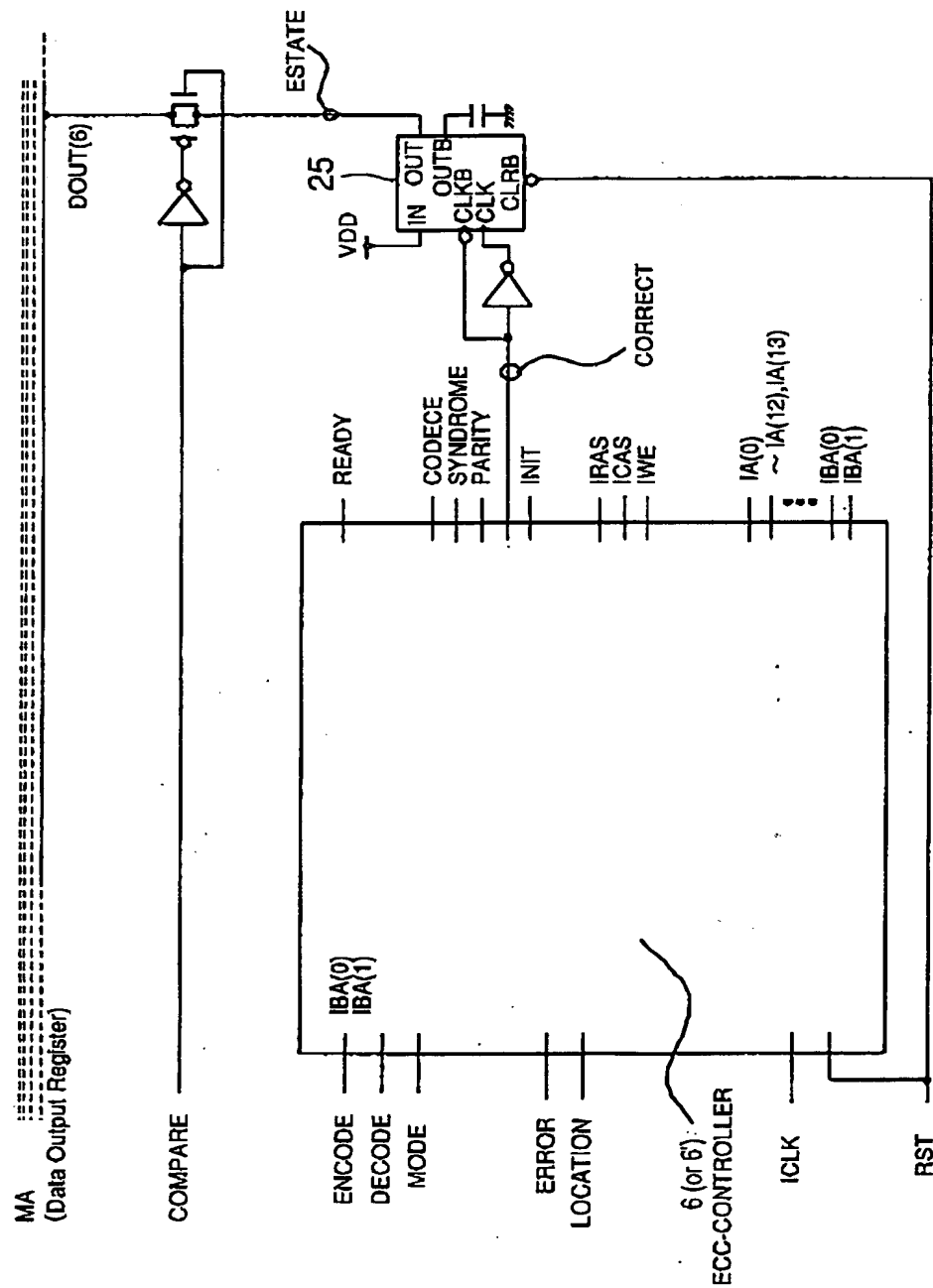


FIG. 16

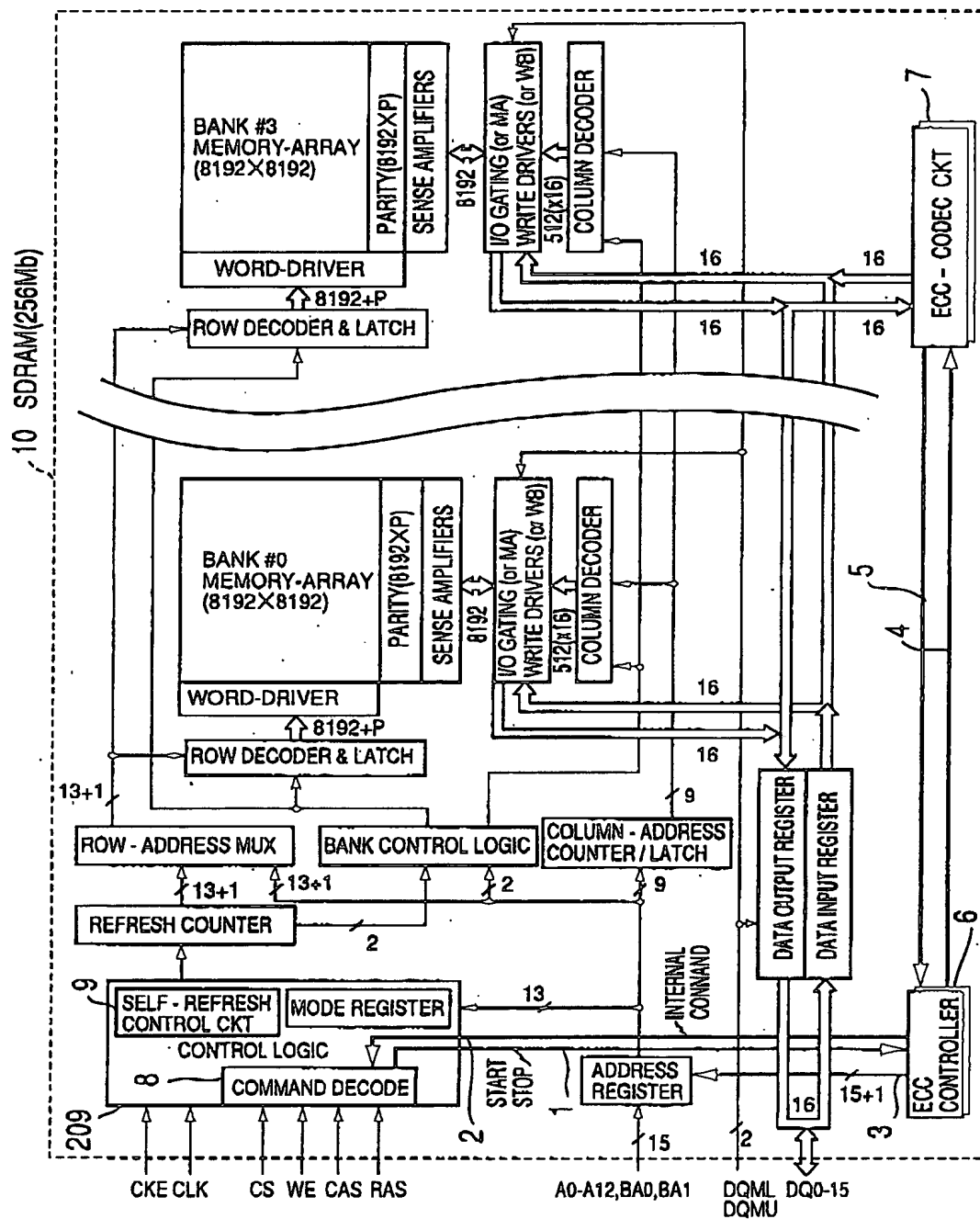
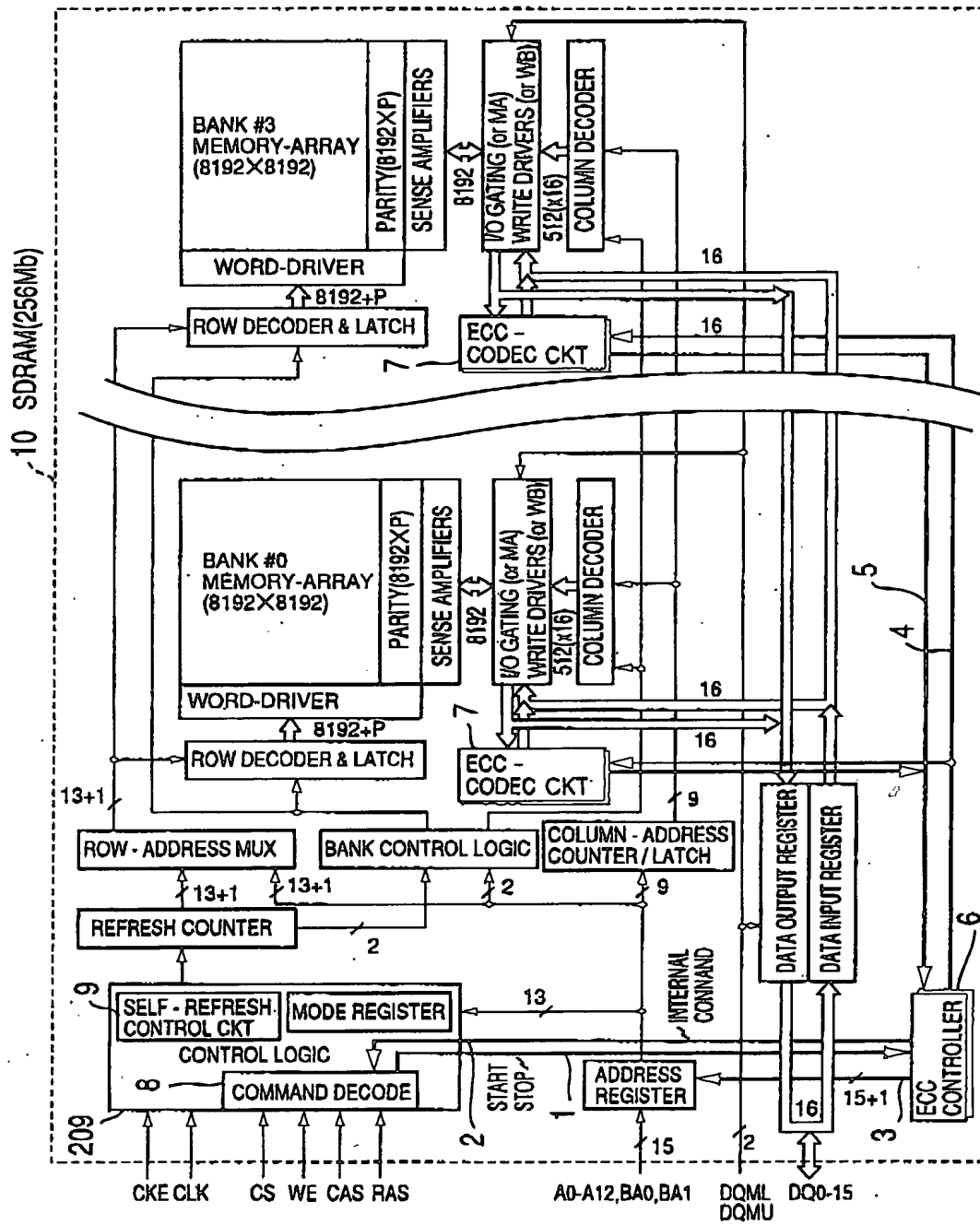
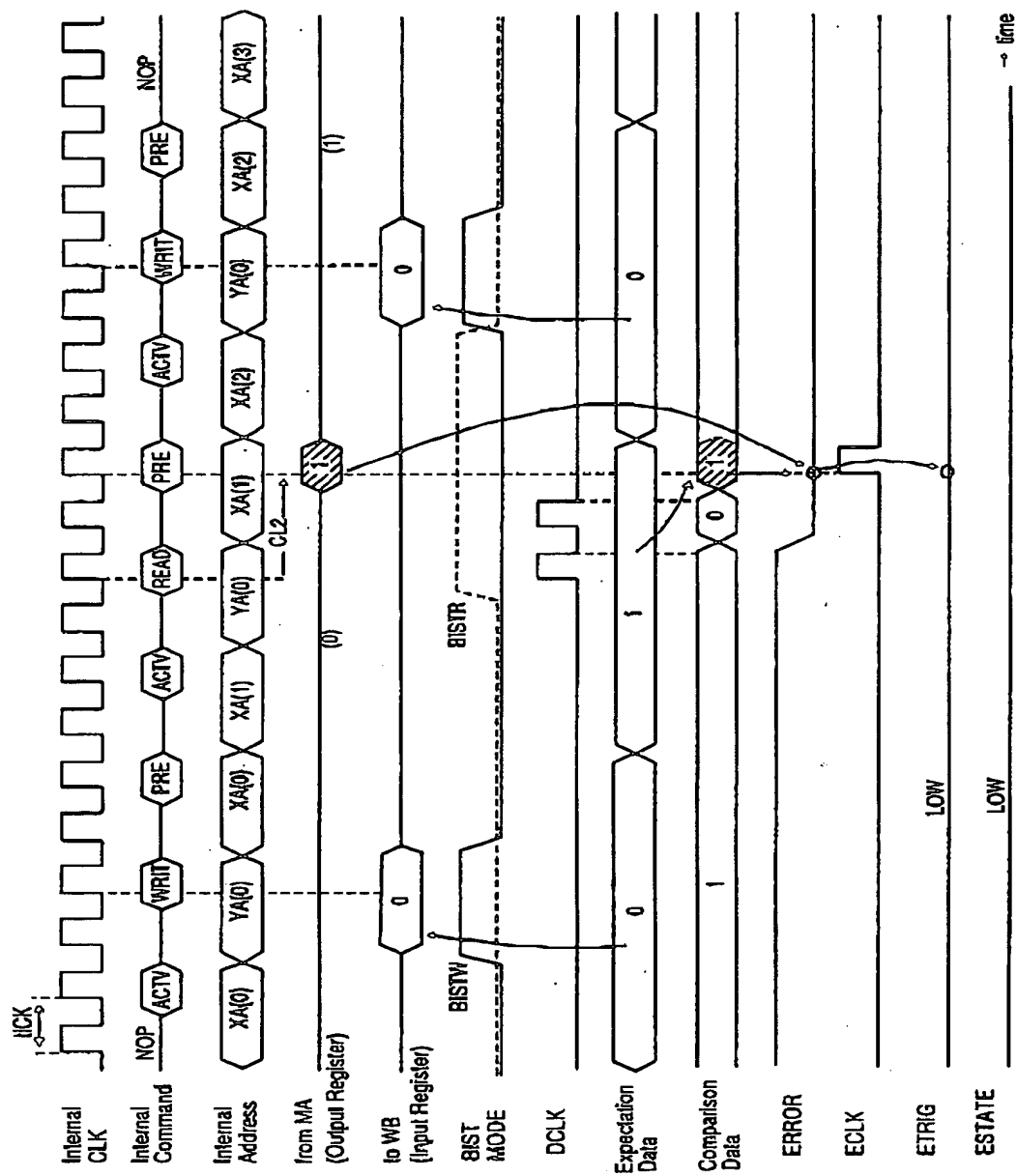


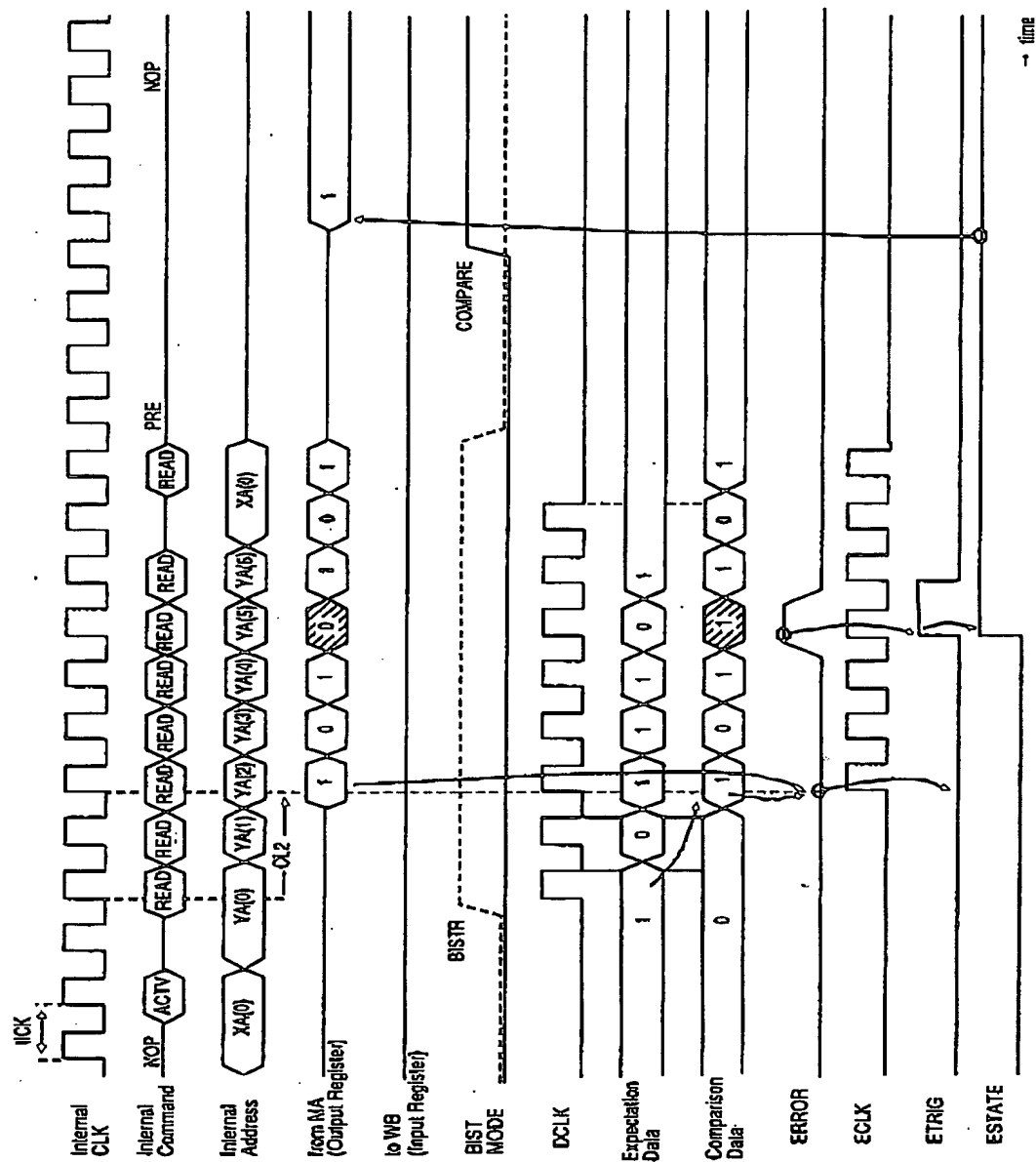
FIG. 17



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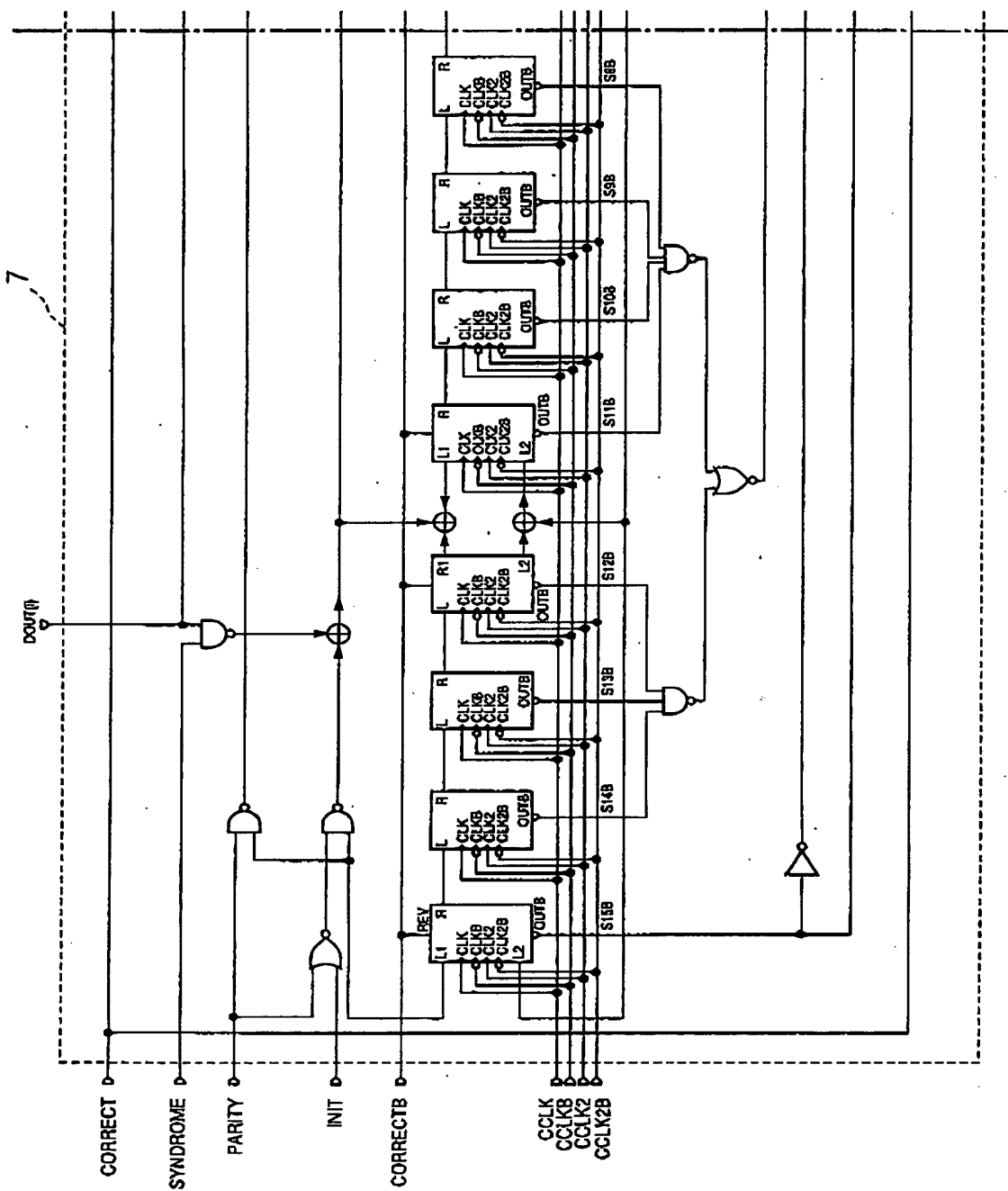


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Example 2 of Self-Test Operation
(Burst Operation, Occurrence of Error, Reading of Result)

FIG. 20



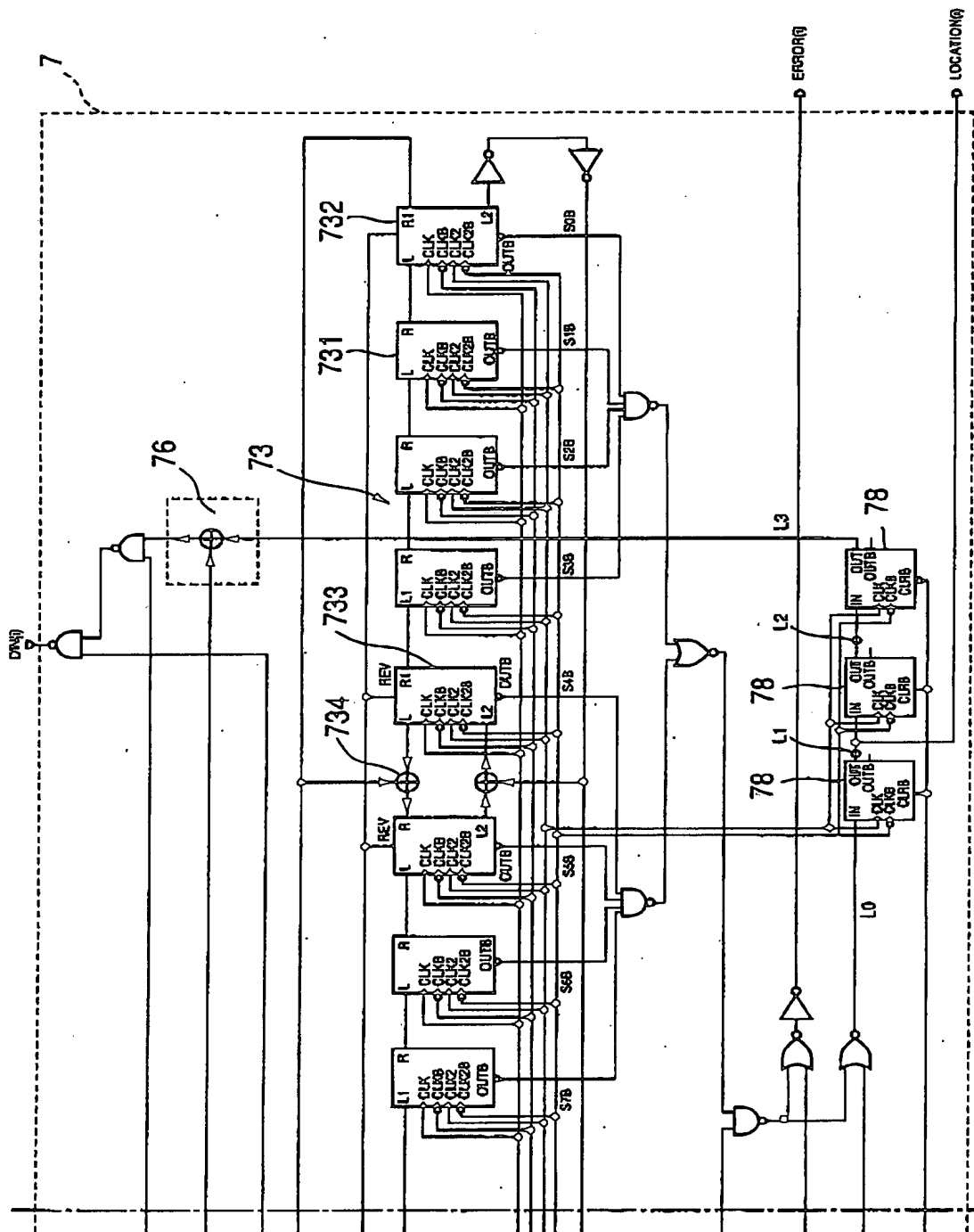


FIG. 22

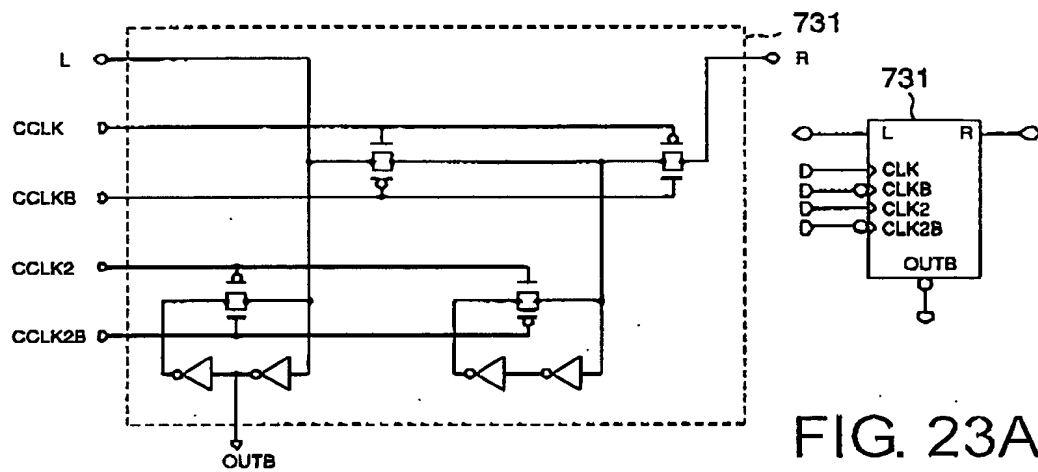


FIG. 23A

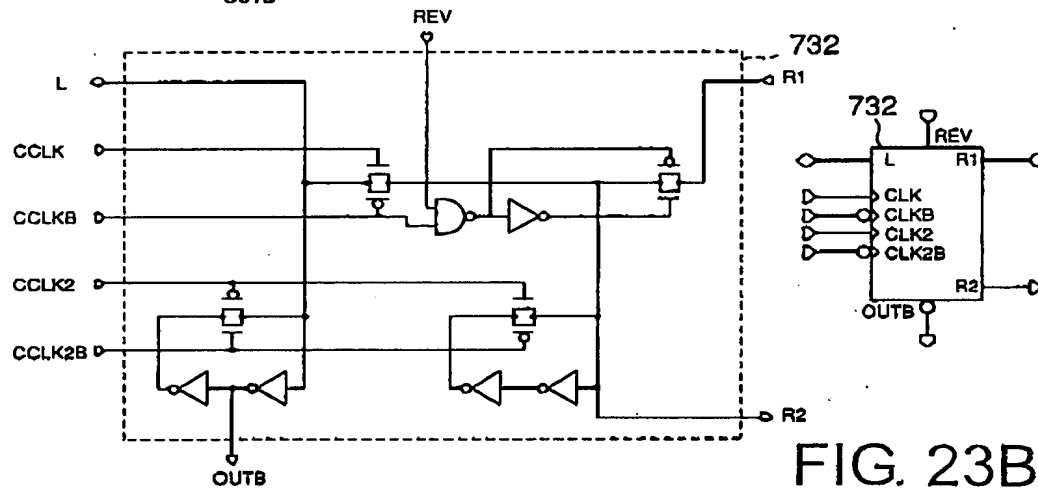


FIG. 23B

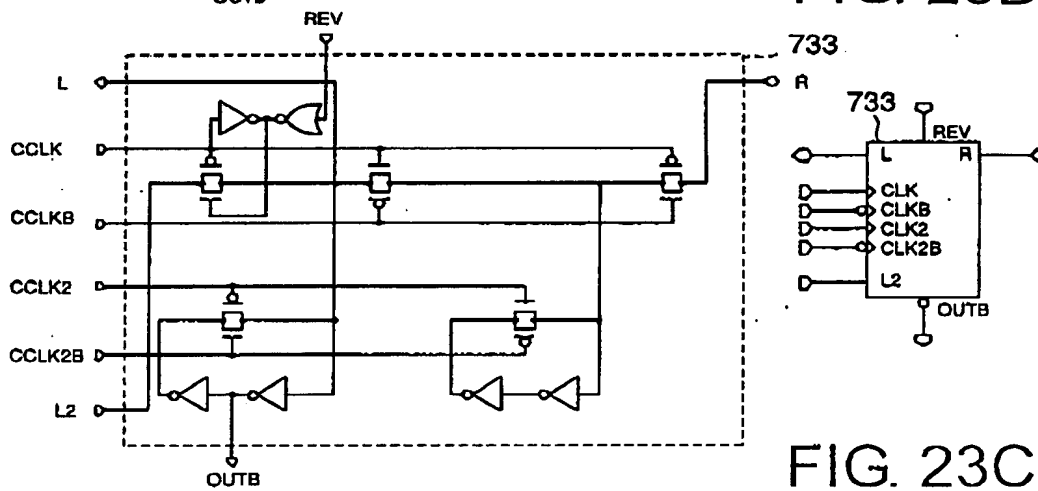


FIG. 23C

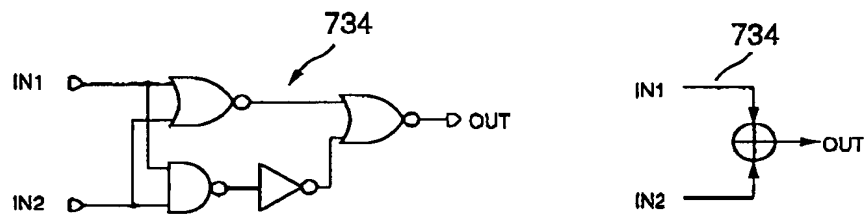


FIG. 24

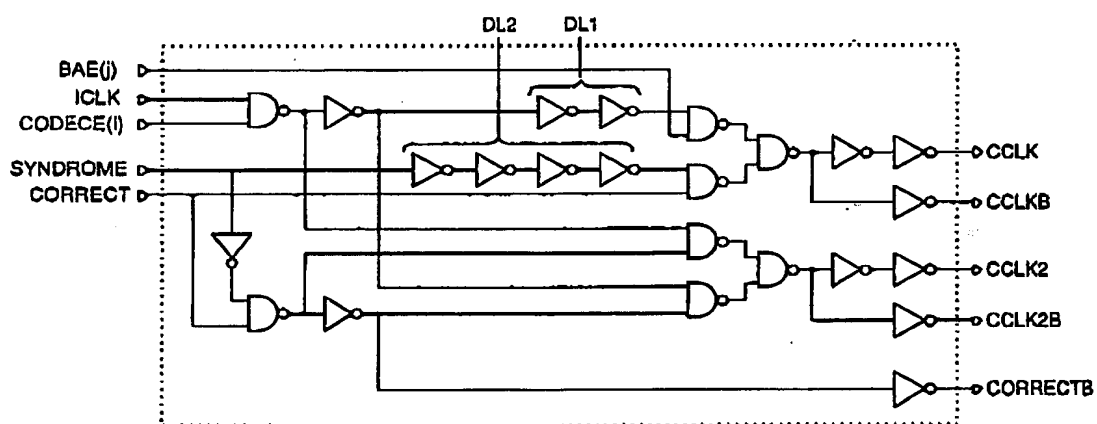
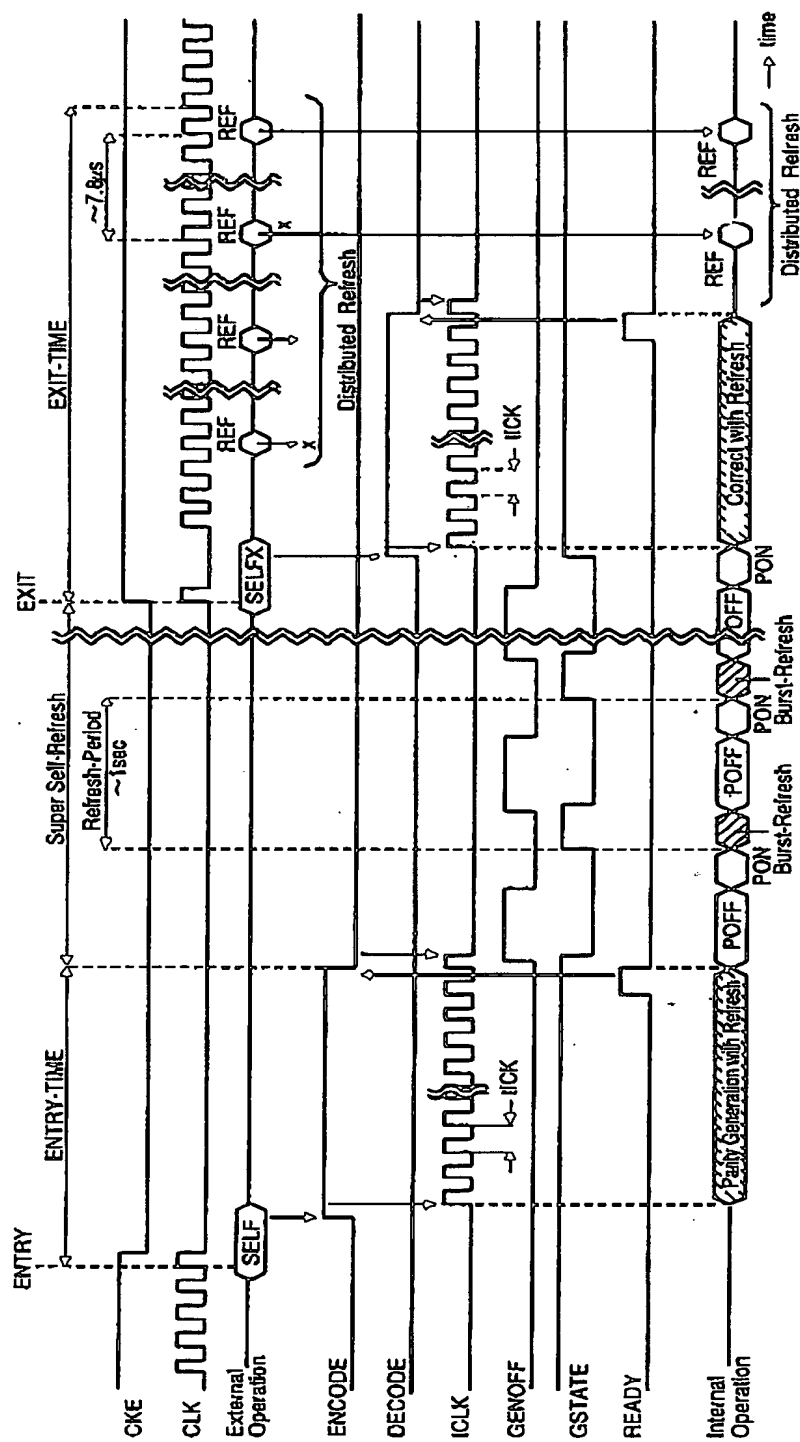


FIG. 25



Sequence of Super Self-Refresh Operation (Entry/Exit Scheme)

FIG. 26

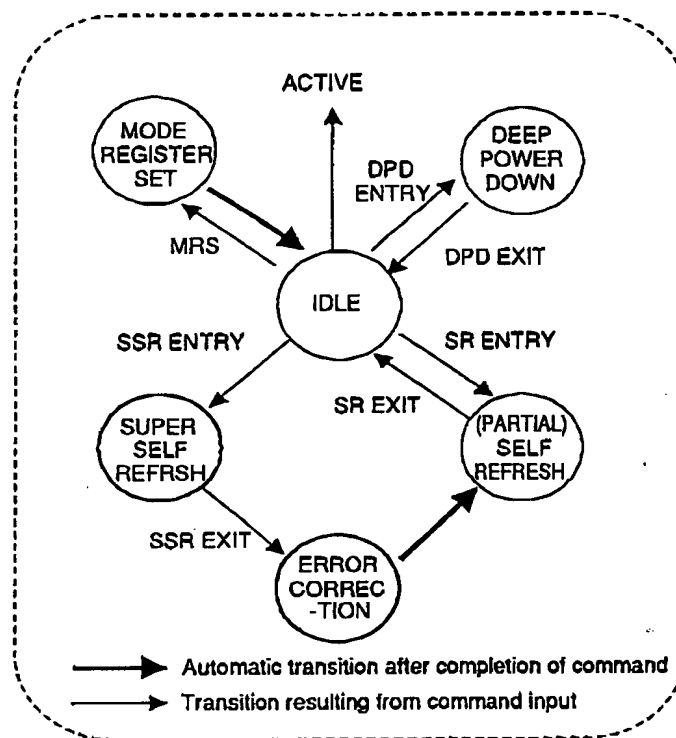


FIG. 27

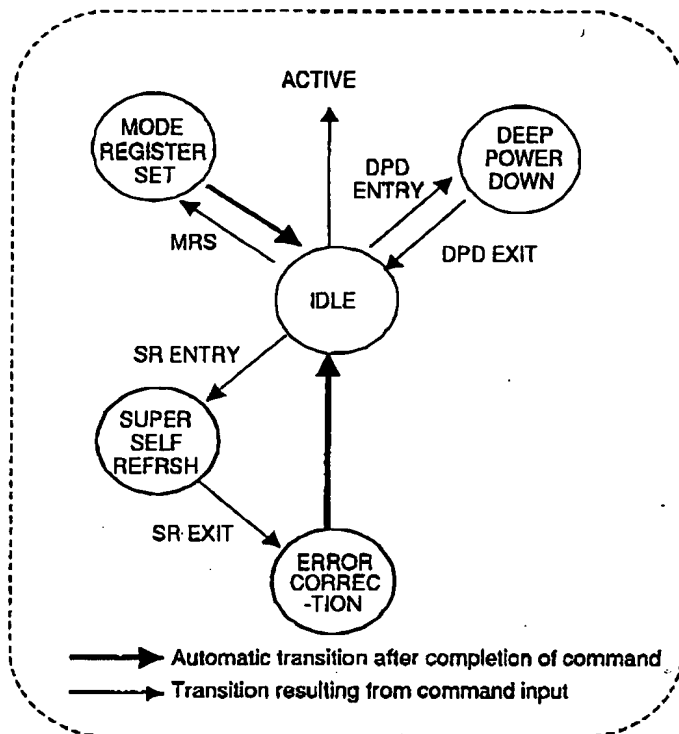


FIG. 28

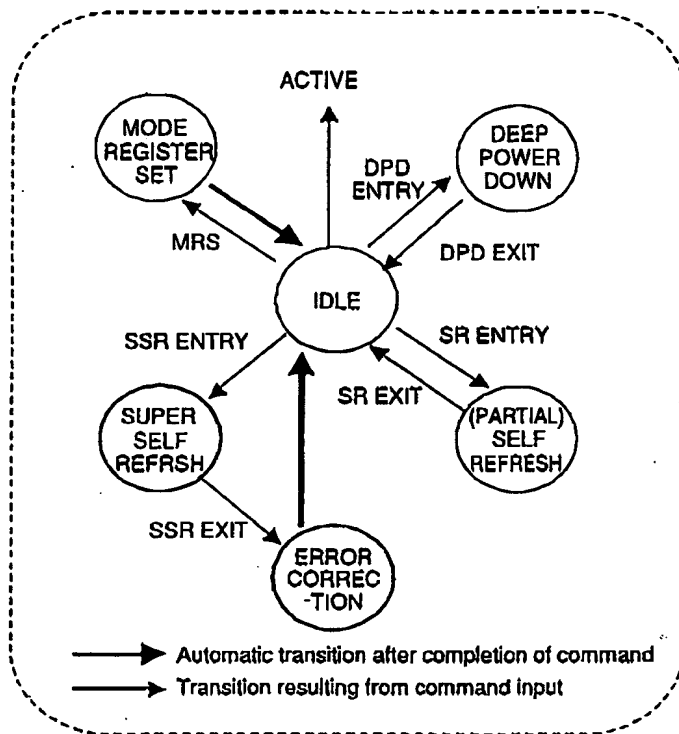


FIG. 29

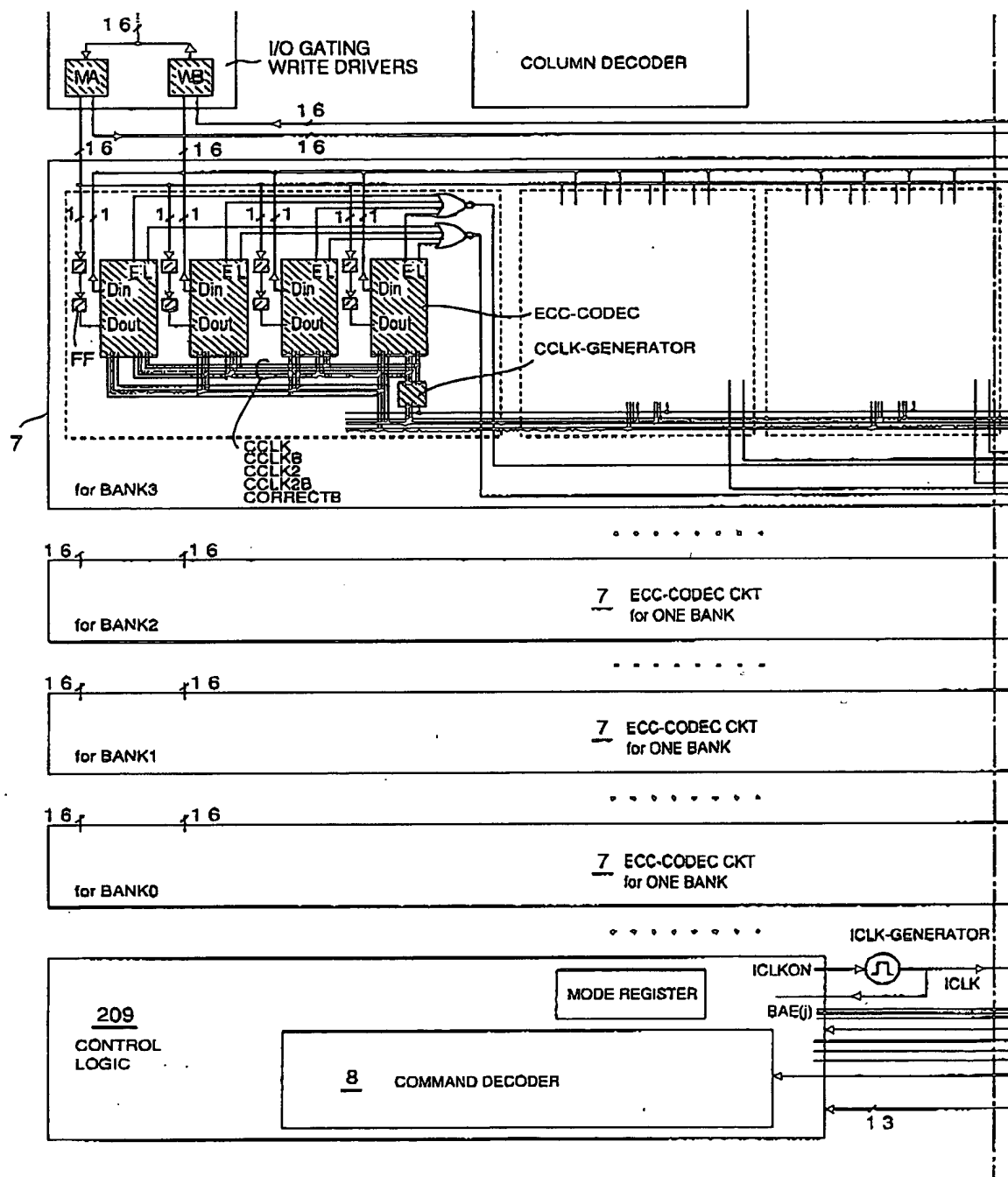


FIG. 30

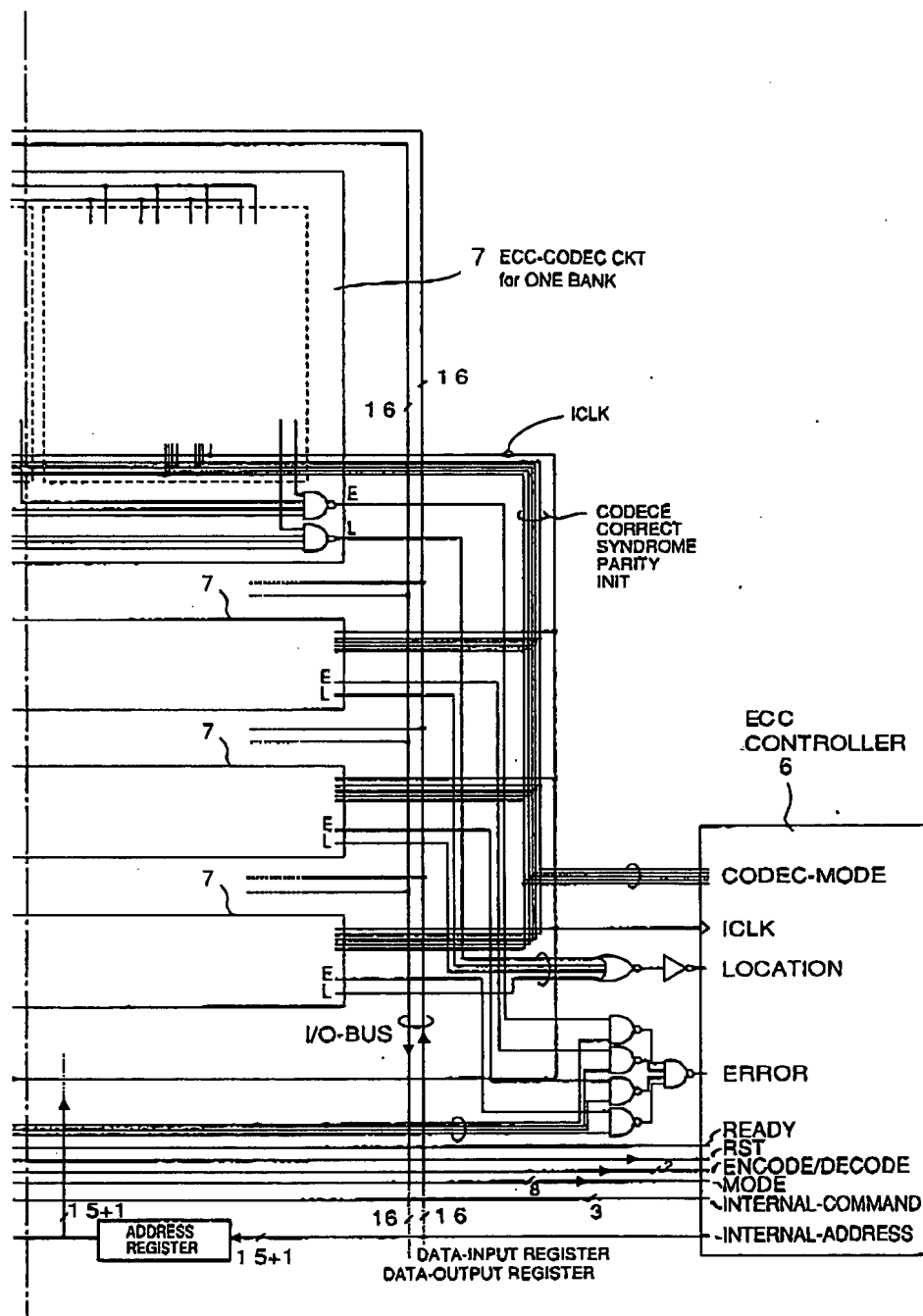


FIG. 31

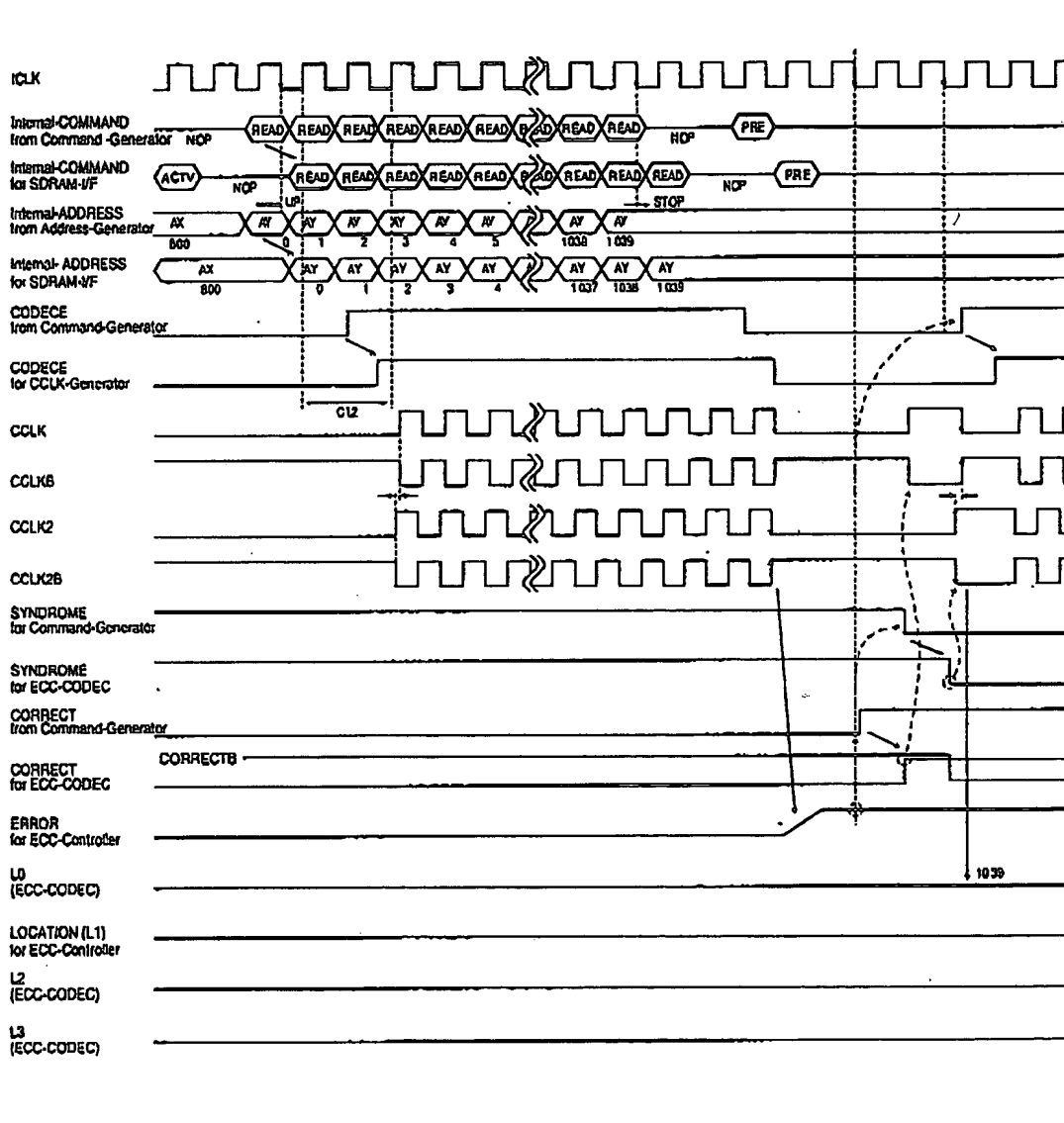


FIG. 32

